CLAIMS

What is Claimed is:

1. A semiconductor device having a surface, comprising:

a first well region of a first conductivity formed beneath said surface;

a second well region of said first conductivity formed beneath said surface;

a region of a second conductivity formed beneath said surface, wherein said region is located between said first well region and said second well region; and

a plurality of conductive sub-surface regions of said first conductivity each formed beneath said first and second well regions in one of a first parallel orientation and a second parallel orientation to form a sub-surface mesh structure, and wherein said sub-surface mesh structure is diagonally positioned relative to said first and second well regions such that a first plurality of conductive boundaries are formed between said first well region and said sub-surface mesh structure and a second plurality of conductive boundaries are formed between said second well region and said sub-surface mesh structure to provide a plurality of sub-surface conductive paths between said first and second well regions without isolating said region.

2. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has an N-type doping.

3. The semiconductor device as recited in Claim 2 wherein said first well region has an N-type doping, and wherein said second well region has an N-type doping.

4. The semiconductor device as recited in Claim 3 wherein said first well region includes a p-type MOSFET (metal oxide semiconductor field effect transistor), and wherein said second well region includes a p-type MOSFET.

5. The semiconductor device as recited in Claim 4 wherein said region has a P-type doping, and wherein said region includes an N-type MOSFET (metal oxide semiconductor field effect transistor).

6. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has a P-type doping.

7. The semiconductor device as recited in Claim 6 wherein said first well region has a P-type doping, and wherein said second well region has a P-type doping.

8. The semiconductor device as recited in Claim 7 wherein said first well region includes an N-type MOSFET (metal oxide semiconductor field effect transistor), and wherein said second well region includes an N-type MOSFET.

9. The semiconductor device as recited in Claim 8 wherein said region has an N-type doping, and wherein said region includes a P-type MOSFET (metal oxide semiconductor field effect transistor).

10. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has a strip shape.

11. The semiconductor device as recited in Claim 1 wherein said sub-surface mesh structure routes a body-bias voltage to said first and second well regions.

12. The semiconductor device as recited in Claim 1 wherein said sub-surface mesh structure is rotated approximately 45 degrees relative to said first well region.

13. The semiconductor device as recited in Claim 1 wherein said sub-surface mesh structure is rotated approximately 45 degrees relative to said second well region.

14. The semiconductor device as recited in Claim 1 wherein an area of said sub-surface mesh structure is equally divided between said conductive sub-surface regions of said first conductivity and a gap area.

15. The semiconductor device as recited in Claim 1 further comprising a second sub-surface layer of said second conductivity formed beneath said sub-surface mesh structure, wherein a gap between adjacent parallel conductive sub-surface

regions is sufficiently wide to avoid pinching-off a conductive path between said region and said second sub-surface layer.

16. A semiconductor device having a surface, comprising:

a first well region of a first conductivity formed beneath said surface;

a second well region of said first conductivity formed beneath said surface;

a region of a second conductivity formed beneath said surface, wherein said region is located between said first well region and said second well region; and

a plurality of conductive sub-surface regions of said first conductivity each formed beneath said first and second well regions in a first parallel orientation, wherein said first parallel orientation is diagonal relative to said first and second well regions such that a first plurality of conductive boundaries are formed between said first well region and said conductive sub-surface regions and a second plurality of conductive boundaries are formed between said second well region and said conductive sub-surface regions to provide a plurality of sub-surface conductive paths between said first and second well regions without isolating said region.

17. The semiconductor device as recited in Claim 16 wherein each conductive sub-surface region has an N-type doping.

18. The semiconductor device as recited in Claim 17 wherein said first well region has an N-type doping, and wherein said second well region has an N-type doping.

19. The semiconductor device as recited in Claim 18 wherein said first well region includes a p-type MOSFET (metal oxide semiconductor field effect transistor), and wherein said second well region includes a p-type MOSFET.

20. The semiconductor device as recited in Claim 19 wherein said region has a P-type doping, and wherein said region includes an N-type MOSFET (metal oxide semiconductor field effect transistor).

21. The semiconductor device as recited in Claim 16 wherein each conductive sub-surface region has a P-type doping.

22. The semiconductor device as recited in Claim 21 wherein said first well region has a P-type doping, and wherein said second well region has a P-type doping.

23. The semiconductor device as recited in Claim 22 wherein said first well region includes an N-type MOSFET (metal oxide semiconductor field effect transistor), and wherein said second well region includes an N-type MOSFET.

24. The semiconductor device as recited in Claim 23 wherein said region has an N-type doping, and wherein said region includes a P-type MOSFET (metal oxide semiconductor field effect transistor).

25. The semiconductor device as recited in Claim 16 wherein each conductive sub-surface region has a strip shape.

26. The semiconductor device as recited in Claim 16 wherein said conductive sub-surface regions route a body-bias voltage to said first and second well regions.

27. The semiconductor device as recited in Claim 16 wherein said first parallel orientation and said first well region form an angle that is approximately 45 degrees.

28. The semiconductor device as recited in Claim 16 wherein said first parallel orientation and said second well region form an angle that is approximately 45 degrees.

29. The semiconductor device as recited in Claim 16 further comprising a second sub-surface layer of said second conductivity formed beneath said conductive sub-surface regions, wherein a gap between adjacent parallel conductive sub-surface regions is sufficiently wide to avoid pinching-off a conductive path between said region and said second sub-surface layer.

30. A semiconductor device having a surface, comprising:

a first well region of a first conductivity formed beneath said surface;

a second well region of said first conductivity formed beneath said surface;

a region of a second conductivity formed beneath said surface, wherein said region is located between said first well region and said second well region; and

a plurality of conductive sub-surface regions of said first conductivity each formed beneath said first and second well regions in one of a first parallel orientation and a second parallel orientation to form a sub-surface mesh structure, and wherein said sub-surface mesh structure is axially positioned relative to said first and second well regions such that a first plurality of conductive boundaries are formed between said first well region and said sub-surface mesh structure and a second plurality of conductive boundaries are formed between said second well region and said sub-surface mesh structure to provide a plurality of sub-surface conductive paths between said first and second well regions without isolating said region.

31. The semiconductor device as recited in Claim 30 wherein each conductive sub-surface region has an N-type doping.

32. The semiconductor device as recited in Claim 31 wherein said first well region has an N-type doping, and wherein said second well region has an N-type doping.

33. The semiconductor device as recited in Claim 32 wherein said first well region includes a p-type MOSFET (metal oxide semiconductor field effect transistor), and wherein said second well region includes a p-type MOSFET.

34. The semiconductor device as recited in Claim 33 wherein said region has a P-type doping, and wherein said region includes an N-type MOSFET (metal oxide semiconductor field effect transistor).

35. The semiconductor device as recited in Claim 30 wherein each conductive sub-surface region has a P-type doping.

36. The semiconductor device as recited in Claim 35 wherein said first well region has a P-type doping, and wherein said second well region has a P-type doping.

37. The semiconductor device as recited in Claim 36 wherein said first well region includes an N-type MOSFET (metal oxide semiconductor field effect transistor), and wherein said second well region includes an N-type MOSFET.

38. The semiconductor device as recited in Claim 37 wherein said region has an N-type doping, and wherein said region includes a P-type MOSFET (metal oxide semiconductor field effect transistor).

39. The semiconductor device as recited in Claim 30 wherein each conductive sub-surface region has a strip shape.

40. The semiconductor device as recited in Claim 30 wherein said sub-surface mesh structure routes a body-bias voltage to said first and second well regions.

41. The semiconductor device as recited in Claim 30 wherein said first parallel orientation is parallel to said first well region, and wherein said second parallel orientation is perpendicular to said first well region.

42. The semiconductor device as recited in Claim 30 wherein said first parallel orientation is parallel to said second well region, and wherein said second parallel orientation is perpendicular to said second well region.

43. The semiconductor device as recited in Claim 30 wherein an area of said sub-surface mesh structure is equally divided between said conductive sub-surface regions of said first conductivity and a gap area.

44. The semiconductor device as recited in Claim 30 further comprising a second sub-surface layer of said second conductivity formed beneath said sub-surface mesh structure, wherein a gap between adjacent parallel conductive sub-surface regions is sufficiently wide to avoid pinching-off a conductive path between said region and said second sub-surface layer.

45. A semiconductor device having a surface, comprising:

a first well region of a first conductivity formed beneath said surface;

a second well region of said first conductivity formed beneath said surface;

a region of a second conductivity formed beneath said surface, wherein said region is located between said first well region and said second well region; and

a plurality of conductive sub-surface regions of said first conductivity each formed beneath said first and second well regions in a first parallel orientation, wherein said first parallel orientation is perpendicular relative to said first and second well regions such that a first plurality of conductive boundaries are formed between said first well region and said conductive sub-surface regions and a second plurality of conductive boundaries are formed between said second well region and said conductive sub-surface regions to provide a plurality of sub-surface conductive paths between said first and second well regions without isolating said region.

46. The semiconductor device as recited in Claim 45 wherein each conductive sub-surface region has an N-type doping.

47. The semiconductor device as recited in Claim 46 wherein said first well region has an N-type doping, and wherein said second well region has an N-type doping.

48. The semiconductor device as recited in Claim 47 wherein said first well region includes a p-type MOSFET (metal oxide semiconductor field effect transistor), and wherein said second well region includes a p-type MOSFET.

49. The semiconductor device as recited in Claim 48 wherein said region has a P-type doping, and wherein said region includes an N-type MOSFET (metal oxide semiconductor field effect transistor).

50. The semiconductor device as recited in Claim 45 wherein each conductive sub-surface region has a P-type doping.

51. The semiconductor device as recited in Claim 50 wherein said first well region has a P-type doping, and wherein said second well region has a P-type doping.

52. The semiconductor device as recited in Claim 51 wherein said first well region includes an N-type MOSFET (metal oxide semiconductor field effect transistor), and wherein said second well region includes an N-type MOSFET.

53. The semiconductor device as recited in Claim 52 wherein said region has an N-type doping, and wherein said region includes a P-type MOSFET (metal oxide semiconductor field effect transistor).

54. The semiconductor device as recited in Claim 45 wherein each conductive sub-surface region has a strip shape.

55. The semiconductor device as recited in Claim 45 wherein said conductive sub-surface regions route a body-bias voltage to said first and second well regions.

56. The semiconductor device as recited in Claim 45 further comprising a second sub-surface layer of said second conductivity formed beneath said conductive sub-surface regions, wherein a gap between adjacent parallel conductive sub-surface regions is sufficiently wide to avoid pinching-off a conductive path between said region and said second sub-surface layer.